ORIGINAL ARTICLE

An Effective Power Management Circuit system for Energy Harvesting Applications

Chun-Chang Wu, Yu-Jie Huang, Yi-Cheng Chiou, Yu-Hao Chen, and Shey-Shi Lu*

Department of Electrical Engineering, National Taiwan University, Taiwan

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*Corresponding author: sslu@ntu.edu.tw

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Abstract: A high-efficiency power management circuit is realized using TSMC 0.35μm CMOS process to convert energy harvested from the environment for battery storage as a suitable power supply for application circuitry. A high conversion efficiency (74%) switching voltage regulator is designed to serve as a digital control circuit with greater tolerance to power noise. For noise-sensitive analog circuits such as amplifiers and the analog-to-digital converters, a linear low dropout (LDO) regulator is also designed to provide a cleaner and more stable power supply. In addition, a microcontroller which can effectively control the power switching of each circuit block is also implemented. To prevent power waste, the system blocks normally stay in standby mode with extremely low power consumption. Each block will be turned on only when instructed to activate.

Keywords: DC/DC converter; MCU; PMU; LDO

Introduction

The rapid development of information technologies and semiconductor production processes has greatly reduced production costs for electronic products, making them affordable to the general public. Now, the increasing miniaturization and portability of consumer electronic products has focused attention on battery limitations. Batteries need to be recharged or replaced after a few hours use, requiring users to prepare spare batteries or power cords. Thus consumers today demand products that offer longer usage time per charge, without compromising product size.

Repeated charging and discharging of off–the–shelf energy storage components like rechargeable batteries and supercapacitors can result in inconsistent output voltages and voltage fluctuation. Therefore, to suppress this voltage source instability, this paper proposes a power management system which can efficiently convert the voltage output of batteries into an optimal and stable power source to supply application circuitry [1]. Furthermore, to avoid excessive energy wastage, a digital microcontroller with power management is also designed to manage the switching of each sub-circuit.

System Architecture

An efficient power management circuit system is realized using TSMC 0.35μm standard CMOS process, with simulations conducted using Cadence Circuit Design Software. Figure 1 illustrates the whole system architecture consisting of a buck switching regulator, a

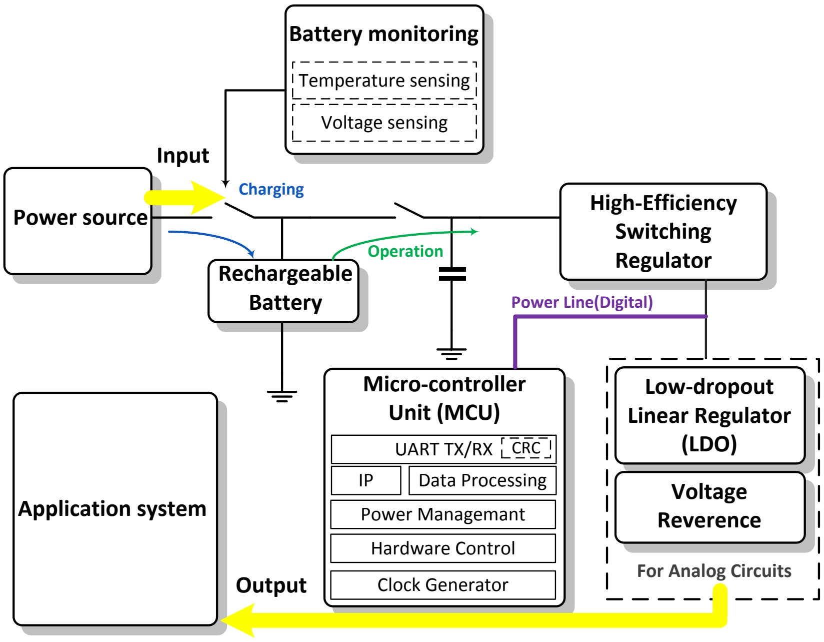

Figure 1. Block diagram of the proposed system.

low dropout regulator (LDO), battery monitoring circuits, and an microcontroller unit (MCU) with energy management [2, 3]. The buck-type switching regulator circuit, which has high energy conversion efficiency, is adopted to lower output voltage from batteries [4]. The generated output voltage will be a little bit noisy due to continuous switching. This voltage is then fed directly into digital circuits like MCUs, which are have a higher tolerance for noise from the power supply. However, the noise may interfere with normal analog circuit performance, so a linear low dropout (LDO) regulator is added to reduce noise and provide the analog circuits with a cleaner and more stable power supply. To maximize energy efficiency, we designed a microcontroller with power management to control the power switching of the sub-blocks throughout the system.

Chun-Chang Wu is a Ph.D. candidate in electronic engineering at National Taiwan University. His research interests include ultra-low power, energy harvesting and energy efficient power management circuits.

Yu-Jie Huang is a Ph.D. candidate in electronic engineering at National Taiwan University. His research interests include CMOS mixed-signal integrated circuit design and system- on-a-chip design for wireless sensing and biomedical applications.

Yi-Cheng Chiou received his M.S. degrees in electrical engineering from National Taiwan University in 2013. His research interests include analog and mixed-signal circuit design, wireless communication, energy harvesting, and biomedical applications.

Yu-Hao Chen is an M.S. candidate in electronic engineering at National Taiwan University. His research interests include analog and mixed-signal circuit design and biomedical applications.

Shey-Shi Lu received his Ph.D. in electrical engineering from the University of Minnesota, Minneapolis-St. Paul in 1991. In August 1991, he joined the Department of Electrical Engineering at National Taiwan University, where he currently serves as Professor. His research interests are in the areas of RF integrated circuits (RFICs)/monolithic microwave integrated circuits (MMICs) and micromachined RF components.

The system's default status is standby mode, thus reducing the power consumption. In this mode, energy obtained from the environment exceeds energy consumed by the system, thus keeping the battery charged. When the system receives a command signal, the blocks are activated. The system uses a battery for energy storage, thus we also design a battery monitor circuit to monitor battery conditions (e.g., temperature voltage, etc.), thus preventing system damage from overcharging or overheating. Below we describe each circuit block in detail.

Buck Switching Regulator

The following application circuitry has relatively low power consumption, thus it does not impose much of a load on the proposed system. To save energy, PFM modulation control is applied to increase the conversion efficiency. Figure 2 shows the basic principle of the switching buck regulator. When the switch SW is in the conduction state, the voltage of (V_{IN}-V_{OUT}) will be across the inductor L, and the inductor current will increase at a rate of (V_{IN}-V_{OUT})/L. When the switch SW is turned off, since the inductor current cannot change rapidly, the diode will be forced on, thus enabling the inductor current to go into the load. The voltage across the inductor is V_{OUT} at this time, but in an opposite polarity, so the inductor current decreases with a slope of -V_{OUT}/L. The relation between output voltage and input voltage is $V_{out} = V_{IN} \times d$, where d is the duty cycle ($d = \frac{t_{on}}{t_{on} + t_{off}}$) of the switching control signal. The structure of the buck circuit is different from the boost structure, and the output current of the buck circuit is always the same as the inductor current. Figure 3 shows a schematic diagram of a PFM buck converter. The control circuit is composed of a hysteresis comparator and a ring oscillator. The output voltage is divided by R1 and R2, and the divided voltage is compared with a voltage reference V_{REF}. The stable average output voltage is $V_{out} = V_{REF}\left(1+\frac{R2}{R1}\right)$.

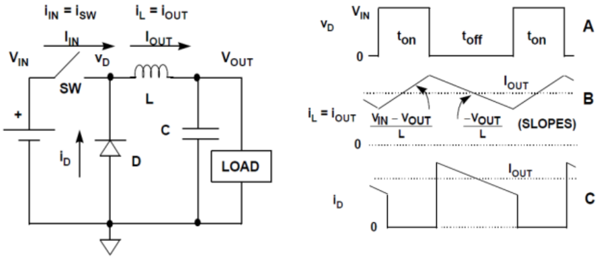

Figure 2. The basic principle of switching buck regulator.

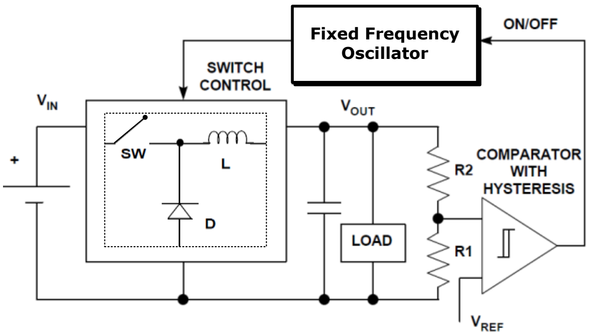

Figure 3. Schematic of the proposed PFM buck converter.

Low Dropout Regulator (LDO)

The output voltage of switching buck converters is typically quite noisy, so an LDO is designed to provide a relatively clean power source for the system's analog circuit. The main purpose of the LDO is to regulate the output voltage, not for voltage tuning. The larger the difference between the LDO's output and input voltages, the lower its efficiency, so the output voltage is designed to be as close to the input voltage as possible to maximize power efficiency. Also, the input signals for the RF receiver and the front-end amplifier circuit are weak and thus require a very stable voltage source to minimize interference from the power supply. To confront the temperature variation, a bandgap reference voltage circuit is introduced.

Figure 4 shows the regulator circuit. The current is mainly provided by a large PMOS transistor. To provide a stable voltage source V_{out}, the gate of the power PMOS is controlled by an error amplifier. One end of the error amplifier is connected to the bandgap reference to provide a stable voltage source V_{REF}, while the other end is connected to the divided voltage VFB. Since the inputs of the error amplifier are the gates of the input devices, there is no current between V_{FB} and the error amplifier feedback path, which means $VFB = V_{out} \bullet \frac{R2}{R1+R2}$. Since PMOS forms a negative feedback path through R1 and R2, VFB is forced to be equipotential to V_{REF}, and finally becomes $V_{out} = V_{REF}(1+\frac{R2}{R1})$. This result shows that there is no relation between V_{in} and V_{out}, so the voltage source provided by the regulator can be isolated from the interference of the voltage source. In addition, V_{REF} is formed by the bandgap reference voltage of the circuit, thus making V_{out} also insensitive to temperature variation. As shown in Figure 4, the error amplifier here is designed to be a two stage amplifier circuit, compensated by the Miller RC.

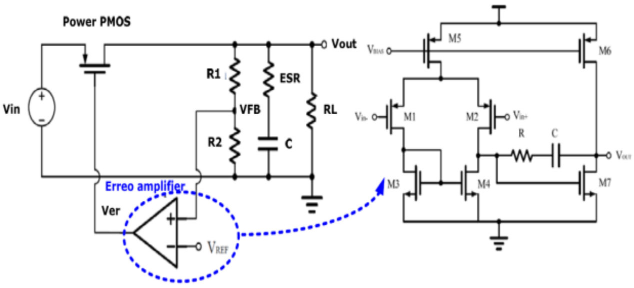

Figure 4. Schematic of the proposed LDO.

Battery Monitoring Circuit

The structure of the proposed battery monitoring circuit is shown in Figure 5. It consists of a battery temperature sensor and a battery voltage sensor. The temperature sensor was developed by our team for other projects. As for voltage sensing, the battery voltage value can be measured simply using a voltage divider, then comparing it the result with a reference voltage. Based on the result of the comparator, the back-end control circuit decides whether to cut off the battery connection to prevent the system from over-heating, or to remind users to recharge or replace the battery.

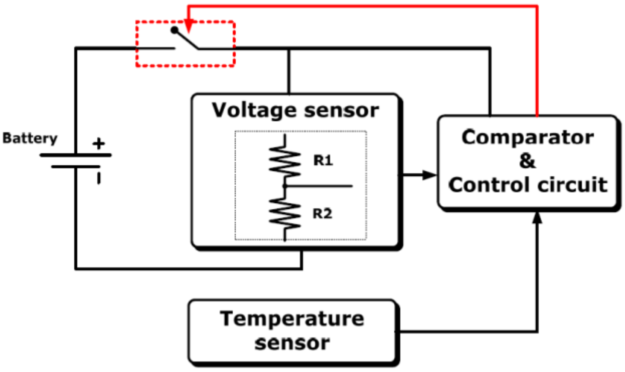

Figure 5. Schematic of the proposed battery monitoring circuits.

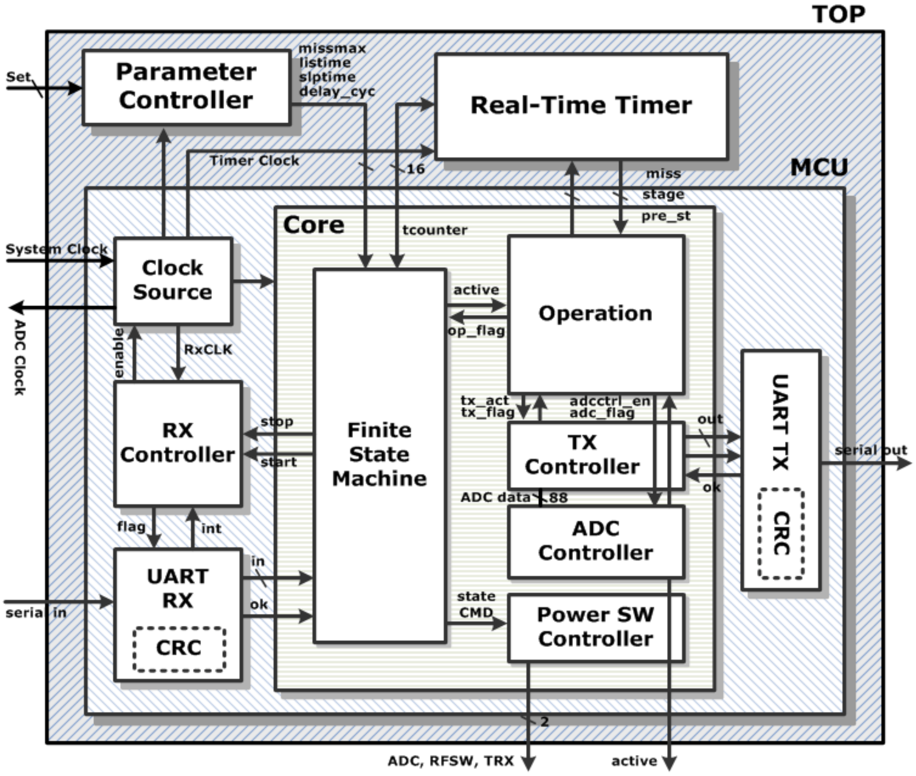

Figure 6. Schematic of the proposed MCU.

Power Management Microcontroller (MCU)

This paper proposes a microcontroller designed specifically for near field communications applications. The microcontroller is capable of hardware control, standby power savings, error detection, and communication data processing. The main features of the MCU are:

1. Simple functions, focusing mainly on “management” with minimal calculations.
2. Error detection and correction of the transmitted data.
3. Receiving the data from the receiver circuit and pass it to the transmitter circuit.
4. Differentiating degree of signal correctness.
5. Executing the command signal, controlling the data flow.
6. Power-saving management (in sleep mode only leak current is consumed).
7. Peripheral circuit control (triggering and cutting off sensors, amplifiers, ADC, transceivers, antennas, etc.)

The circuit structure is shown in Figure 6.

Measurements

Buck Switching Regulator

Figure 7 shows the conversion efficiency with respect to the load of the buck switching regulator circuit. The efficiency of the circuit under heavy loading (R_{Load} <1kΩ) is about 65%, while under light loading (1kΩ ~ 100kΩ) the energy efficiency ranges widely between 10 ~ 75%, and is generally worse than under heavy loading. The highest energy conversion efficiency point of the buck regulator circuit occurs when the load is 1kΩ, which can be up to 74%, while the output power is about 0.13mW.

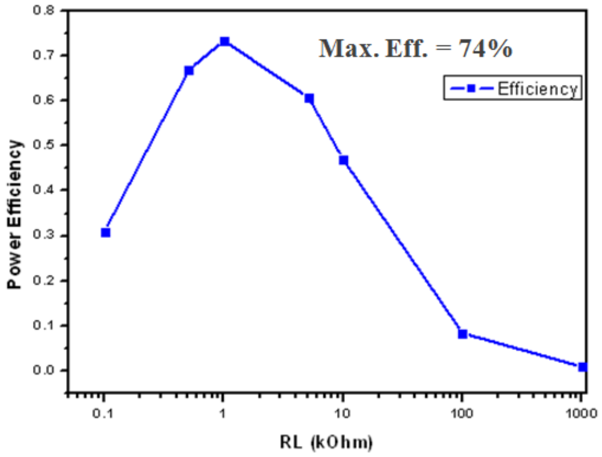

Figure 7. The conversion efficiency and load measurement chart of the switch buck regulator circuit.

Low Dropout Regulator : LDO

Figure 8 shows the conversion efficiency with respect to the load of the linear low dropout regulator (LDO). The output efficiency is not high when the circuit is under heavy loading (RLoad <0.5 kΩ). However, when the circuit is under light loading (1 kΩ nearby), the energy efficiency can rise as high as 80 ~ 90%. The highest efficiency (~89%) of the linear low-dropout regulator occurs at 1 kΩ load.

Figure 9 shows the conversion efficiency with respect to the load of the buck regulator and the linear low dropout regulator (LDO). The highest efficiency (77.2%) occurs at 0.51 kΩ load.

The die photo of the proposed power management system is shown in Figure 10. The system parameters and design arrangements are shown in Table 1.

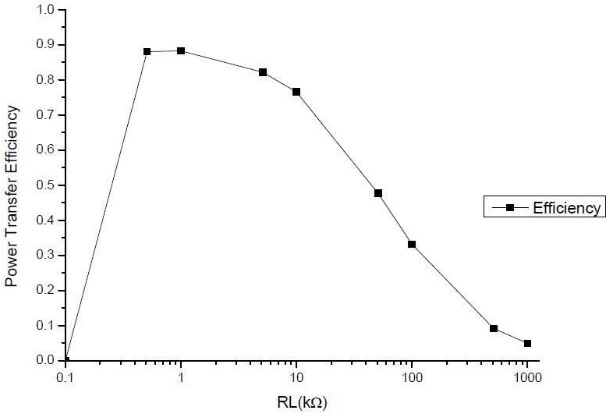

Figure 8. The conversion efficiency and load measurement chart of the linear low dropout regulator (LDO).

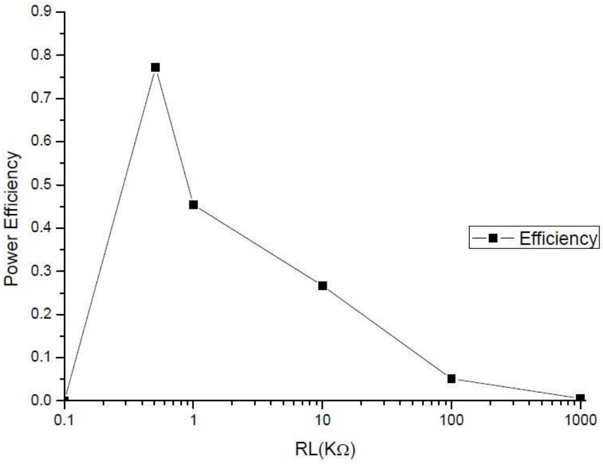

Figure 9. The conversion efficiency and load measurement chart of the switch,buck regulator circuit and linear low dropout regulator (LDO).

Table 1. System parameters and design arrangement.

Technology	TSMC 0.35µm CMOS
DC/DC type	PFM /switching regulator, LDO
Battery monitoring circuits	Battery Temp. & voltage
Power management circuit	MCU

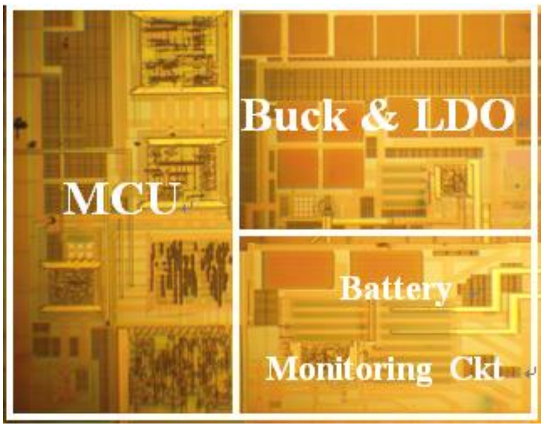

Figure 10. Proposed power management system die photo.

Conclusion

This paper proposes a high-efficiency power management SoC implemented using the TSMC 0.35µm standard CMOS process. The system can shut down temporarily unused circuit blocks to reduce unnecessary power consumption. The maximum conversion efficiency of the buck switching converter and linear low dropout regulator (LDO) was 77.2%. Moreover, the system is set in low power consumption standby mode by default and circuit blocks only work when the wake-up signal is received, thus significantly decreasing power loss. This power-saving feature is in line with broader trends in technology R&D, specifically for CPUs and cloud technology, etc. The proposed power management system can be used in a wide range of applications.

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